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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,163	09/17/2003	Chien-Chang Huang	4392-0137P	4184

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EXAMINER	
MANDALA, VICTOR A	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,163	HUANG ET AL.	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: Figure 1 #s 112 & 114 and Figure 3 #s 324, 326, 328, and 334. Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,798,545 Iwasa et al.

2. Referring to claim 1, a test structure for use in DRAM comprising: a semiconductor substrate, (Figure 2 #1); a transistor, (Figure 2 examiner's label #300), formed on said semiconductor substrate, (Figure 2 #1), said transistor, (Figure 2 examiner's label #300), comprising a first region, (Figure 2 #16), and a second region, (Figure 2 #15), both said first region, (Figure 2 #16), and said second region, (Figure 2 #15), being formed in said semiconductor substrate, (Figure 2 #1), said first region, (Figure 2 #16), and said second region, (Figure 2 #15), for use as source/drain regions of said transistor, (Figure 2 examiner's label #300); a deep trench capacitor, (Figure 2 examiner's label #400), formed in said semiconductor substrate, (Figure 2 #1), and adjacent to said transistor, (Figure 2 examiner's label #300), said deep trench capacitor, (Figure 2 examiner's label #400), having a first width, (Figure 2 examiner's label #W1), a shallow trench insulator (STI) , (Figure 2 examiner's label #200 the area of the insulator that fills the trench between #6s of the capacitor), formed in a top portion of said deep trench capacitor, (Figure 2 examiner's label #400), said STI, (Figure 2 examiner's label #200), having a second width, (Figure 2 examiner's label #W2), wherein said second width, (Figure 2 examiner's label #W2), is substantially shorter than said first width, (Figure 2 examiner's label #W1); a third region, (Figure 2 examiner's label #100), formed in said semiconductor substrate, (Figure 2 #1), and adjacent to said deep trench capacitor, (Figure 2 examiner's label #400); a first contact, (Figure 2 #17), formed on said semiconductor substrate, (Figure 2 #1), and contacting with said first region, (Figure 2 #16); and a second contact, (Figure 2 #14 the one directly above examiner's label #100 in the center of the Figure), formed on said semiconductor substrate, (Figure 2 #1), and contacting with said third region, (Figure 2 examiner's label #100).

3. Referring to claim 2, a test structure, wherein said semiconductor substrate, (Figure 2 #1), is a silicon substrate, (Col. 4 Line 51).

4. Referring to claim 3, a test structure, wherein said transistor, (Figure 2 examiner's label #300), comprises a gate, said gate comprises a silicon oxide layer, (Figure 2 #8 Col. 5 Lines 30-34), formed on said semiconductor substrate, (Figure 2 #1), and an electric conductor layer formed, (Figure 2 #9), on said silicon oxide layer, (Figure 2 #8).

5. Referring to claim 4, a test structure, further comprising two gate contacts, (Figure 2 examiner's label #500 & #9), formed on said semiconductor substrate, (Figure 2 #1), and located on said deep trench capacitor, (Figure 2 examiner's label #400).

6. Referring to claim 5, a test structure, wherein said gate contact comprising a silicon oxide layer, (Figure 2 #7 Col. 5 Lines 18), formed on said semiconductor substrate, (Figure 2 #1), and an electric conductor layer, (Figure 2 examiner's label #500 & #9), formed on said silicon oxide layer, (Figure 2 #7 Col. 5 Lines 18).

7. Referring to claim 6, a test structure, wherein said electric conductor layer, (Figure 2 #9), is a metal silicide layer, (Col. 6 Lines 53-54).

8. Referring to claim 7, a test structure, wherein said first region, (Figure 2 #16), said second region, (Figure 2 #15), and said third region, (Figure 2 examiner's label #100), are formed by doping a dopant, (Col. 6 Lines 55-56), into said semiconductor substrate, (Figure 2 #1).

9. Referring to claim 8, a test structure for use in DRAM, (Col. 3 Lines 15-16), comprising: a silicon substrate, (Figure 2 #1 Col. 4 Line 51); a transistor, (Figure 2 examiner's label #300), formed on said silicon substrate, (Figure 2 #1), said transistor, (Figure 2 examiner's label #300),

comprising a first region, (Figure 2 #16), and a second region, (Figure 2 #15), both said first region, (Figure 2 #16), and said second region, (Figure 2 #15), being formed in said silicon substrate, (Figure 2 #1 Col. 4 Line 51), said first region, (Figure 2 #16), and said second region, (Figure 2 #15), for use as source/drain regions of said transistor, (Figure 2 examiner's label #300); a deep trench capacitor, (Figure 2 examiner's label #400), formed in said silicon substrate, (Figure 2 #1 Col. 4 Line 51), and adjacent to said transistor, (Figure 2 examiner's label #300), said deep trench capacitor, (Figure 2 examiner's label #400), having a first width, (Figure 2 examiner's label #W1); a shallow trench insulator (STI) , (Figure 2 examiner's label #200), formed in a top portion of said deep trench capacitor, (Figure 2 examiner's label #400), said STI, (Figure 2 examiner's label #200), having a second width, (Figure 2 examiner's label #W2), and said second width, (Figure 2 examiner's label #W2), being substantially shorter than said first width, (Figure 2 examiner's label #W1); two gate contacts, (Figure 2 examiner's label #500 & #9), formed on said silicon substrate, (Figure 2 #1 Col. 4 Line 51), and located on said deep trench capacitor, (Figure 2 examiner's label #400), and said two gate contacts, (Figure 2 examiner's label #500 & #9), being separated by said STI, (Figure 2 examiner's label #200); a buried strap, (Figure 2 examiner's label #100), formed in said silicon substrate, (Figure 2 #1), and adjacent to said deep trench capacitor, (Figure 2 examiner's label #400); a first contact, (Figure 2 #17), formed on said silicon substrate, (Figure 2 #1 Col. 4 Line 51), and contacting with said first region, (Figure 2 #16); a second contact, (Figure 2 #14 the one directly above examiner's label #100 in the center of the Figure), formed on said silicon substrate, (Figure 2 #1 Col. 4 Line 51), and contacting with said buried strap, (Figure 2 examiner's label #100).

10. Referring to claim 9, a test structure, wherein said transistor, (Figure 2 examiner's label #300), comprises a gate, said gate comprises a silicon oxide layer, (Figure 2 #8 Col. 5 Lines 30-34), formed on said semiconductor substrate, (Figure 2 #1), and an electric conductor layer formed, (Figure 2 #9), on said silicon oxide layer, (Figure 2 #8).

11. Referring to claim 10, a test structure, wherein said gate contact comprising a silicon oxide layer, (Figure 2 #7 Col. 5 Lines 18), formed on said silicon substrate, (Figure 2 #1 Col. 4 Line 51), and an electric conductor layer, (Figure 2 examiner's label #500 & #9), formed on said silicon oxide layer, (Figure 2 #7 Col. 5 Lines 18).

12. Referring to claim 11, a test structure, wherein said electric conductor layer, (Figure 2 #9), is a metal silicide layer, (Col. 6 Lines 53-54).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
6/18/04